I CLAIM:

1. A memory control system comprising:

a memory controller

a memory device connected to said memory controller via a command bus, wherein command signals are directed from said memory controller to said memory device, said memory device comprising:

one or more memory banks;

a row address register;

a command decoder that is connected to said row address register and receives said command signals and controls the contents of said row address register; and

a refresh circuit connected to said one or more memory banks and said row address register, wherein said refresh circuit avoids unnecessary power consumption for refreshing said one or more memory banks.

2. The memory control system of claim 1, wherein said refresh circuit only refreshes a range of rows of said one or more memory banks based on a predetermined value stored in said row address register.

3. The memory control system of claim 1, wherein said row address register stores a predetermined value representative of the maximum row address of said one or more memory banks that receives a write command from said command signals.

4. The memory control system of claim 1, wherein said row address register stores a predetermined value representative of the minimum row address of said one or more memory banks that receives a write command from said command signals.

5. The memory control system of claim 2, wherein said row address register stores a predetermined value representative of the maximum row address of said one or more memory banks that receives a write command from said command signals; and said refresh circuit only refreshes rows of said one or more memory banks that have addresses less than or equal to said predetermined value.

6. The memory control system of claim 2, wherein said row address register stores a predetermined value representative of the minimum row address of said one or more memory banks that receives a write command from said command signals; and said refresh circuit only refreshes rows of said one or more memory banks that have addresses greater than or equal to said predetermined value.

7. The memory control system of claim 1, wherein said memory controller comprises a normal refresh circuit that sends an autorefresh signal to said memory device via said command bus.

8. The memory control system of claim 1, wherein said refresh circuit comprises:

a refresh address counter for incrementing a row address to be refreshed during a refresh cycle; and

a controller that controls access to a row address requested to be refreshed by a refresh request.

9. The memory control system of claim 1, wherein said refresh circuit performs refreshing as part of an autorefresh operation.

10. The memory control system of claim 1, wherein said refresh circuit performs refreshing as part of a self-refresh operation.

11. The memory control system of claim 1, wherein said memory controller comprises a normal refresh circuit.

12. A memory control system comprising:

a memory controller

a memory device connected to said memory controller via a command bus, wherein command signals are directed from said memory controller to said memory device, said memory device comprising:

one or more memory banks;

a first row address register;

a second row address register

a command decoder that is connected to said first row address register and said second row address register and receives said command signals and controls the contents of said first row address register and said second row address register; and

a refresh circuit connected to said one or more memory banks and said row address register, wherein said refresh circuit avoids unnecessary power consumption for refreshing said one or more memory banks.

13. The memory control system of claim 12, wherein said refresh circuit only refreshes a range of rows of said one or more memory banks based on a first predetermined value stored in said first row address register and a second predetermined value stored in said second row address register.

14. The memory control system of claim 13, wherein said first predetermined value is representative of the maximum row address of said one or more memory banks that receive a write command from said command signals.

15. The memory control system of claim 13, wherein said first predetermined value is representative of the minimum row address of said memory banks that receive a write command from said command signals.

16. The memory control system of claim 13, wherein said refresh circuit only refreshes rows of said one or more memory banks that have addresses less than or equal to said first predetermined value and greater than or equal to said second predetermined value.

17. The memory control system of claim 12, wherein said memory controller comprises a normal refresh circuit that sends an autorefresh signal to said memory device via said command bus.

18. The memory control system of claim 12, wherein said refresh circuit comprises:

a refresh address counter for incrementing a row address to be refreshed during a refresh cycle; and

a controller that controls access to a row address requested to be refreshed by a refresh request.

19. The memory control system of claim 12, wherein said refresh circuit performs refreshing as part of an autorefresh operation.

20. The memory control system of claim 12, wherein said refresh circuit performs refreshing as part of a self-refresh operation.

21. A memory control system comprising:

a memory controller

a memory device connected to said memory controller via a command bus, wherein command signals are directed from said memory controller to said memory device, said memory device comprising:

two or more memory banks;

one row address register for each of said two or more memory banks;

a command decoder that is connected to row address register and receives said command signals and controls the contents of said row address register; and

a refresh circuit connected to said two or more memory banks and said row address register, wherein said refresh circuit avoids unnecessary power consumption for refreshing said two or more memory banks.

22. The memory control system of claim 21, wherein said refresh circuit only refreshes a range of rows of said two or more memory banks based on predetermined values stored in said row address registers corresponding to said two or more memory banks.

23. The memory control system of claim 21, wherein each of said row address registers stores a predetermined value representative of the maximum row address of the corresponding memory bank of said two or more memory banks which was addressed during a write command from said

command signals; and said refresh circuit only refreshes rows of said two or more memory banks that have addresses less than or equal to said predetermined values in the corresponding said address registers.

24. The memory control system of claim 21, wherein each of said row address registers stores a predetermined value representative of the minimum row address of the corresponding memory bank of said two or more memory banks which was addressed during a write command from said command signals; and said refresh circuit only refreshes rows of said two or more memory banks that have addresses greater than or equal to said predetermined values in the corresponding said address registers.

25. The memory control system of claim 21, further comprising a second row address register for each memory bank of said two or more memory banks that is connected to said command decoder and whose contents are controlled by said command decoder; and

wherein said row first address register stores a predetermined value representative of the maximum row address of the corresponding memory bank of said two or more memory banks which was addressed during a write command from said command signals; and said second row address register stores a second predetermined value representative of the minimum row address of the corresponding memory bank of said two or more memory banks which was addressed during a write command from said command signals; and said refresh circuit only refreshes rows of said memory banks

that have addresses less than or equal to said predetermined value and greater than or equal to said second predetermined value in the two corresponding address registers.

26. The memory control system of claim 21, wherein said refresh circuit performs refreshing as part of an autorefresh operation.

27. The memory control system of claim 21, wherein said refresh circuit performs refreshing as part of a self-refresh operation.

28. A method of refreshing several memory banks that receive command signals from a memory controller, the method comprising:

monitoring command signals received by a memory device; and

refreshing said several memory banks based on said monitored command signals so as to avoid unnecessary power consumption for refreshing said several memory banks.

29. The method of claim 28, wherein said monitoring comprises determining whether or not a write command is received by said several memory banks of said memory device and indicating that said several memory banks contains data stored therein.

30. The method of claim 28, wherein said monitoring comprises determining a maximum row address for each of said several memory banks of said memory device that receives a write command; and

performing said refreshing based on said determined maximum row address.

31. The method of claim 28, wherein said monitoring comprises determining a minimum row address for each of said several memory banks of said memory device that receives a write command; and

performing said refreshing based on said determined minimum row address.

32. The method of claim 30, wherein said monitoring comprises determining a minimum row address of said memory that receives a write command; and

performing said refreshing based on said determined minimum row address.

33. The method of claim 28, wherein said refreshing is a self-refreshing operation.

34. The method of claim 28, wherein said refreshing is an auto-refreshing operation.